

CLAIMS

1. A printed circuit board having signal vias and ground vias, said printed circuit board comprising:

a first row of vias having a plurality of signal vias;

a second row of vias having a plurality of signal vias, said second row of vias being consecutive with said first row of vias; and

a plurality of rows of vias between said first row of vias and said second row of vias, said plurality of rows of vias being coupled to a ground plane.

2. The printed circuit board of claim 1 wherein said plurality of rows of vias comprises at least one row of vias receiving leads of a component.

3. The printed circuit board of claim 2 wherein said plurality of rows of vias comprises at least one row of vias adjacent said first row of vias.

4. The printed circuit board of claim 3 wherein said plurality of rows of vias comprises at least one row of vias adjacent said second row of vias.

5. The printed circuit board of claim 4 wherein said rows of vias adjacent said first row of vias and said second row of vias comprise vias having a smaller diameter than vias of said at least one of vias receiving leads of a component.

6. The printed circuit board of claim 3 wherein said plurality of rows of vias between said first row of vias and said second row of vias comprises a row of vias receiving a ground lead of a component.

7. A printed circuit board having signal vias and ground vias, said printed circuit board comprising:

a pair of rows of vias having signal vias, said signal vias receiving leads of a component;

a pair of rows of vias having ground vias between said pair of rows of vias having signal vias; and

a row of vias having ground vias between said pair of rows of vias having ground vias, said ground vias receiving other leads of said component.

8. The printed circuit board of claim 7 wherein said pair of rows of vias having ground vias remains open.

9. The printed circuit board of claim 7 wherein said pair of rows of vias having ground comprises vias having a smaller diameter than said signal vias.

10. The printed circuit board of claim 7 wherein said pair of rows of vias having ground vias provides return current paths for signals in said signal vias.

11. The printed circuit board of claim 7 wherein said pair of rows of vias having ground vias is open.

12. A printed circuit board assembly having signal vias and ground vias, said printed circuit board assembly comprising:

a back plane printed circuit board, said back plane printed circuit board comprising:

a pair of rows of vias having signal vias, said signal vias receiving leads of a connectors;

a pair of rows of vias having ground vias between said pair of rows having signal vias, said pair of rows of vias having ground vias located adjacent rows of vias having signal vias;

a row of vias having ground vias between said pair of rows having ground vias and receiving other leads of said connectors; and

a plurality of connectors; and
a plurality of printed circuit boards having corresponding connectors, said plurality of printed circuit being coupled to said connectors of said back plane printed circuit board by way of said plurality of corresponding connectors.

13. The printed circuit board of claim 12 wherein said plurality of printed circuit boards comprises a plurality of integrated circuit packages.

14. The printed circuit board of claim 12 wherein said backplane printed circuit board and said plurality of printed circuit boards form a switch for routing digital data.

15. The printed circuit board of claim 12 wherein said pair of rows of vias having ground vias comprises vias having a smaller diameter than said signal vias.

16. The printed circuit board of claim 12 wherein said pair of rows of vias having ground vias provides return current paths for signals in said signal vias.

17. A method of reducing cross talk in a printed circuit board, said method comprising the steps of:

providing a plurality of rows of signal vias coupling predetermined leads of a plurality of components to signal vias of said plurality of rows of said signal vias;

coupling ground leads of said plurality of components to a plurality of rows of ground vias; and

providing a return path for signals on said signal vias by way of rows of ground vias adjacent to said rows of signal vias.

18. The method of claim 17 further comprising a step of providing said plurality of rows of ground vias having vias

of a diameter to receive leads of said plurality of components.

19. The method of claim 18 further comprising a step of providing rows of ground vias, adjacent said rows of signal vias, having a diameter less than the diameter of said vias of said plurality of rows of ground vias.

20. The method of claim 19 further comprising a step of coupling a second printed circuit board to a component of said plurality of components.

21. The method of claim 17 further comprising a step of providing high speed communication signals by way of said printed circuit board.

22. A method of forming a multi-layer printed circuit board, said method comprising the steps of:

providing a plurality of layers, each layer having traces for routing electrical signals;

forming a first plurality of rows of vias through said plurality of layers, said vias of said first plurality rows having a first diameter; and

forming a second plurality of rows of vias through said plurality of layers, said vias of said second plurality of rows of vias having a second diameter smaller than said first diameter.

23. The method of claim 22 wherein said step of forming a first plurality of rows of vias through said plurality of layers comprises forming vias having a diameter to receive a lead of a component.

24. The method of claim 22 wherein said step of forming a second plurality of rows of vias through said plurality of

layers comprises forming a row of vias adjacent a row of vias of said first plurality of rows of vias.

25. The method of claim 22 wherein said step of forming a first plurality of rows of vias through said plurality of layers comprises forming a row of vias having a first diameter between two rows of vias of said second plurality of rows of vias.

26. The method of claim 22 wherein said step of forming a second plurality of rows of vias through said plurality of layers comprises forming two rows of vias having a second diameter on either side of two rows of vias of said first plurality of rows of vias.